

Topology of technology graphs: Small world patterns in electronic circuits

Ramon Ferrer i Cancho,¹ Christiaan Janssen,¹ and Ricard V. Solé^{1,2,3,*}

¹Complex Systems Research Group, FEN-UPC, Campus Nord, B4-B5, Barcelona 08034, Spain

²Santa Fe Institute, 1399 Hyde Park Road, Santa Fe, New Mexico 87501

³NASA-Associated Astrobiology Institute, CSIC/INTA, Carretera del Ajalvir km 4, Madrid, Spain

(Received 22 May 2001; published 24 September 2001)

Recent theoretical studies and extensive data analyses have revealed a common feature displayed by biological, social, and technological networks: the presence of small world patterns. Here we analyze this problem by using several graphs obtained from one of the most common technological systems: electronic circuits. It is shown that both analogic and digital circuits exhibit small world behavior. We conjecture that the small world pattern arises from the compact design in which many elements share a small, close physical neighborhood plus the fact that the system must define a single connected component (which requires shortcuts connecting different integrated clusters). The degree distributions displayed are consistent with a conjecture concerning the sharp cutoffs associated to the presence of costly connections [Amaral *et al.*, Proc. Natl. Acad. Sci. USA **97**, 11 149 (2000)], thus providing a limit case for the classes of universality of small world patterns from real, artificial networks. The consequences for circuit design are outlined.

DOI: 10.1103/PhysRevE.64.046119

PACS number(s): 89.75.Hc, 05.40.-a

I. INTRODUCTION

A class of disordered networks, the so-called small-world (SW) networks [1,2], has been shown to be widespread in very different contexts, including molecular biology [3,4], neural nets [5], Internet topology [6,7], social and scientific collaboration networks [8–11], ecosystems [12,13], or the human language [14]. The presence of SW patterns might provide new, unsuspected clues to the origins of complex networks and to some of their intrinsic emergent properties. These properties would include their evolvability, robustness against external fluctuations or their fragility against unexpected sources of challenge [15,12]. The observation that some of these systems, with a very different origin, display similar statistical features [7], allows one to develop theoretical models inspired in some methods of statistical mechanics in which the details of the units are not explicitly included.

Electronic circuits can be viewed as networks in which vertices (or nodes) are electronic components (e.g., logic gates in digital circuits and resistors, capacitors, diodes, and so on in analogic circuits) and connections (or edges) are wires in a broad sense. The evolution of electronic circuits underwent two fundamental events for our concerns. First, there is the birth of digital circuits replacing and extending the capabilities of analogic circuits. Second, there is integration, allowing one to reduce the size of electronic equipment maintaining the same functionality. As a result, the construction of larger circuits was favored. As far as we know, no systematic analysis of the resulting topology has been performed.

Using the formalism of graph theory, any of these nets can be described in terms of a graph Ω , defined as a pair, $\Omega = (W, E)$, where $W = \{w_i\}, (i = 1, \dots, N)$ is the set of N nodes and $E = \{\{w_i, w_j\}\}$ is the set of edges or connections

between nodes. Here $\xi_{ij} = \{w_i, w_j\}$ indicates that there is an edge (and thus a link) between nodes w_i and w_j . Two connected nodes are called *adjacent*, and the *degree* of a given node is the number of edges connecting it with other nodes.

The SW pattern can be detected from an analysis of two basic statistical properties: the so called *clustering coefficient* C and the *path length* d . Let us consider a set of links ξ_{ij} ($i, j = 1, \dots, N$), where $\xi_{ij} = 1$ if a link exists and zero otherwise and that the average number of links per node is $\langle k \rangle$. Let us indicate by $\Gamma_i = \{j | \xi_{ij} = 1\}$ the set of nearest neighbors of a node $w_i \in W$. The clustering coefficient for this node is defined as the number of connections between the components $w_j \in \Gamma_i$. By defining

$$\mathcal{L}_i = \sum_{j=1}^N \xi_{ij} \left[\sum_{k \in \Gamma_i; j < k} \xi_{jk} \right], \quad (1)$$

we have $C_v(i) = \mathcal{L}_i / \binom{|\Gamma_i|}{2}$, so that the clustering coefficient is the average over W ,

$$C = \frac{1}{N} \sum_{i=1}^N C_v(i), \quad (2)$$

and measures the average fraction of pairs of neighbors of a node that are also neighbors of each other.

The second measure is easily defined. Given two nodes $w_i, w_j \in W$, let $d_{min}(i, j)$ be the minimum path length connecting these two nodes in Ω . The average path length of a given unit will be

$$d_v(i) = \frac{1}{N} \sum_{j=1}^N d_{min}(i, j), \quad (3)$$

and the path length is $d = \langle d_v(i) \rangle$.

Graphs with a small world structure are highly clustered, but d will be small. Random graphs (where nodes are randomly wired) are not clustered, and also have short d [1]. At

*Email address: ricard@ants.upc.es, sole@santafe.edu

the other extreme, regular lattices, with only nearest-neighbor connections among units, are typically clustered and exhibit long paths. A regular lattice can be transformed into a SW if a small fraction of nodes are rewired to randomly chosen nodes. Thus a small degree of disorder generates short paths (as in the random case) retaining the regular pattern [2]. For random graphs, $C^{rand} \approx \langle k \rangle / N$. For SW graphs, d is close to the one expected from random graphs, d^{rand} , with the same $\langle k \rangle$ and $C \gg C^{rand}$.

An additional property of these graphs is their degree distribution $P(k)$. This is defined as the (normalized) frequency of nodes having k edges. The analysis of different real systems reveals different types of small-world network patterns [8], possibly defining a finite set of universality classes. All of these seem to share a remarkable deviation from what one would expect from a totally random graph. Three different types of distributions were recently suggested to represent most of the observed patterns: (i) scale-free networks, in which $P(k) \approx k^{-\gamma}$; (ii) broad-scale networks, i.e., graphs with sharp cutoffs in their power-law degree distributions $P(k) \approx k^{-\gamma} f(k/k^*)$, where k^* gives the cutoff; and (iii) single-scale distributions (either exponential or Gaussian). These distributions have been suggested to share some non-trivial features with other analogous systems from the theory of critical phenomena [8].

Amaral *et al.* [8] recently conjectured that the shape of these distributions might result from the presence (or absence) of constraints limiting the number of links when connections are costly. In this sense, the presence of exponential decays or sharp cutoffs would be a consequence of costly wiring. Costly wiring should be especially obvious in technological networks in which connections between elements involve hardware. In this context two different types of graphs have been analyzed: the Internet [7,16] and the electric power grid [2,1,8]. In this paper we consider a third, obvious example of a technological network where such constraints should operate: electronic circuits.

This is an especially interesting system for three reasons: (a) It involves a graph in which efficient design relies to a large extent on connecting large groups of elements using different short-range links, and regular clusters connected through a small amount of short cuts. In this sense, they are much closer to the Watts-Strogatz original model than any other system. (b) Since technological innovation has pushed these systems toward minimization of hardware connections, clear deviations from long-tailed distributions should be expected, according to Amaral *et al.*'s conjecture. (c) If relevant topological properties (such as the SW architecture) are present in these circuits, then future design strategies might find ways to optimize their tolerance to failure (which is very high in standard hardware devices).

The paper is organized as follows: In Sec. II we present evidence of such SW patterns in electronic circuits, as well as an analysis of their degree distributions. It is shown that the similarity between electronic circuits and ecological systems might be stronger than been pointed above. Such results and their consequences are outlined in Sec. III.

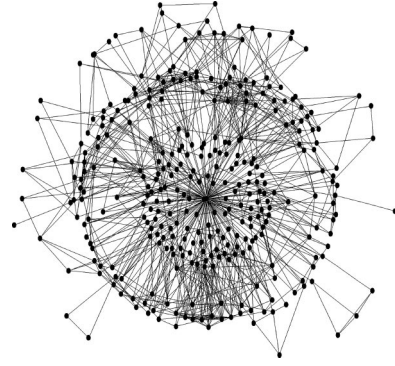


FIG. 1. The graph displayed by an analogic device (old TV circuit) in which each node represents one component (resistors, capacitors, diodes, and so on). Here $N=329$ components define the graph, with an average connectivity $\langle k \rangle=5.12$. This graph has a SW structure, with: $C=0.34 \gg C^{rand}=0.019$ and $d=3.17 \approx d^{rand}=3.13$.

II. RESULTS

We first performed a preliminary analysis of the basic features exhibited by old analogic designs, using available data [17,18]. These networks were used in order to test other types of hypothesis concerning the diversity of different components in a circuit and their average connectivity, to be compared with data from ecological systems. An example of the graph obtained for one of these circuits (a TV circuit) is shown [19] in Fig. 1. We can see that the graph is highly nonrandom, as one would expect from a designed network. Some components are highly connected, but most of them have a small degree. This graph has a SW structure, with $C=0.34 \gg C^{rand}=0.019$ and $d=3.17 \approx d^{rand}=3.13$.

The degree distribution for the three largest networks $N \approx 350$, analyzed in Refs. [17,18], is shown in Fig. 2(A). A characteristic maximum at $k_c=4$ can be seen (with an average connectivity $\langle k \rangle \approx 5$). This is not surprising, since a minimum of two links is typically expected (except for input or output units) and the analogic system is built on a two-dimensional substrate, thus favoring topological arrangements characteristic of a two-dimensional square lattice. The observation of a degree distribution centered around k_c and having a sharp cutoff at $k^* \approx 25-30$ gives support to Amaral *et al.*'s conjecture concerning the limitations imposed by costly wiring. For comparison, we also show (dashed line) the expected distribution for a purely random (Poisson distributed) system with the same average connectivity. It can be seen that the actual distribution strongly deviates from the Poissonian. For small k it is easily understood due to the obvious limitations imposed by the circuit wiring. At larger k , however, it is remarkable to see that the cut off occurs at much higher values. Although these distributions are not long tailed, we indicate the power-law fit gives an exponent $\gamma \approx 2.5$.

Our second set of circuits provides a better understanding of how these graphs are organized in digital circuits. This set contains benchmark circuits (from the so-called ISCAS'89 and ITC'99 sets [20]). The degree distribution of two large logic circuits $N \approx 10^4$ is shown in Fig. 2(c).

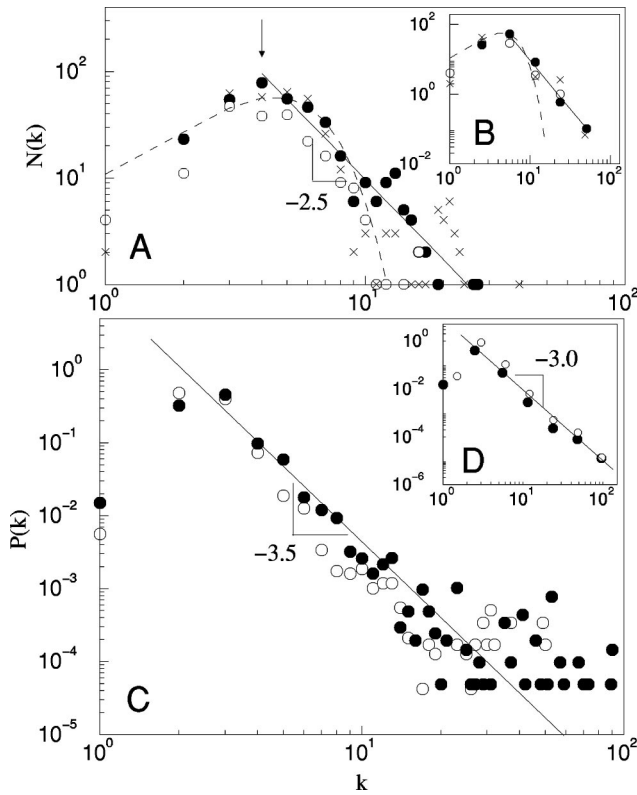


FIG. 2. (a) Degree distribution of three small-sized analogic electronic circuits (three old TV devices); here the three circuits have a size $N \approx 300$ and $\langle k \rangle \approx 5$. A characteristic maximum is observed at $k^+ = 4$, associated with the dominance of four nearest neighbors on a two-dimensional surface (thus defining a two-dimensional lattice of components). A sharp cutoff is also present at $k^* \approx 25 - 30$. In (b) the same distributions are shown using octaves. The expected distributions for a random graph with a Poisson degree distribution and the same average connectivity is also shown (dashed line). It can be seen a clear deviation from the expected random distribution. (c) Degree distributions for two large digital circuits. Here the deviation from the random case is clear, with a tail extending up to a cutoff $k^* \approx 100$; (d) same as (b).

Again, sharp cutoffs are at play, now at larger values. When looking at Fig. 2(d) we again observe the tendency towards a power-law tail with a sharp cutoff. The estimated exponent is close to $\gamma \approx 3$ [21]. It is interesting that this value is close to the one obtained from the Barabási-Albert model [7], and this might have interesting consequences for circuit design (see below).

Circuits in the ISCAS'89/ITC'99 set are formed by components (chiefly gates) having two connections (one input and one output as in NOT gates and D -type flipflops) and three connections (two inputs and one output as in AND2 and OR2 gates). It is straightforward that $\langle k \rangle \geq 2$. If components made use of the minimum number of connections (as it is expected due to optimizations in the logical design), it should be true that $2 \leq \langle k \rangle \leq 3$. In contrast, the value of $\langle k \rangle$ averaged over all the circuits in the ISCAS'89/ITC'99 set is 3.65. All gates have one single output and few inputs. Since an input wire must receive input from only one single output wire (except external input), $\langle k \rangle > 3$ can only be obtained by making a

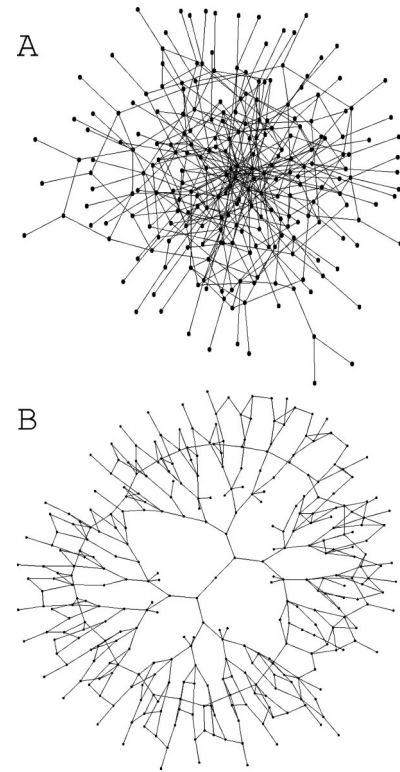


FIG. 3. (a) A lowly clustered logic circuit having $C = 0.0013 < C^{rand} = 0.015$ and $d = 4.33 \approx d^{rand} = 4.22$. The graph has $N = 236$ vertices and $\langle k \rangle = 3.64$. (b) A highly clustered logic circuit having $C = 0.053 > C^{rand} = 0.0099$ and $d = 5.06 \approx d^{rand} = 4.99$. The graph has $N = 320$ vertices, and $\langle k \rangle = 3.175$.

gate to deliver its output to more than one different inputs. The question is why high values of $\langle k \rangle$ (i.e., $\langle k \rangle \gg 4$) are not found. Will such values be redundant in a way that logical optimization cannot tolerate? Is it necessary to go beyond $\langle k \rangle = 3$ for the circuit to perform a nontrivial task? Two predictions from random graph topologies will be used in order to compare them against the observed topological patterns exhibited by the benchmark circuits.

(1) The clustering coefficient over the average connectivity for a random graph follows an inverse scaling law with graph size:

$$\frac{C^{rand}}{\langle k \rangle} = \frac{1}{N} \quad (4)$$

(2) The average path length scales as

$$d^{rand} \log(\langle k \rangle) \approx \log(N). \quad (5)$$

After analyzing 51 logic circuits in the ISCAS'89/ITC'99 set, 25 circuits have $C > C^{rand}$ and 26 circuits have $C < C^{rand}$, from which 17 have $C = 0$. Figures 3(a) and 3(b) show a circuit having $C < C^{rand}$ and another one having $C > C^{rand}$, respectively.

Figure 4 shows the values of $C/\langle k \rangle$ and $d \log \langle k \rangle$ compared to those of $1/N$ and $\log(N)$ for the logic circuits analyzed. It can be seen that $C/C^{rand} > 1$ for most of the circuits. Values of C/C^{rand} of more than one order of

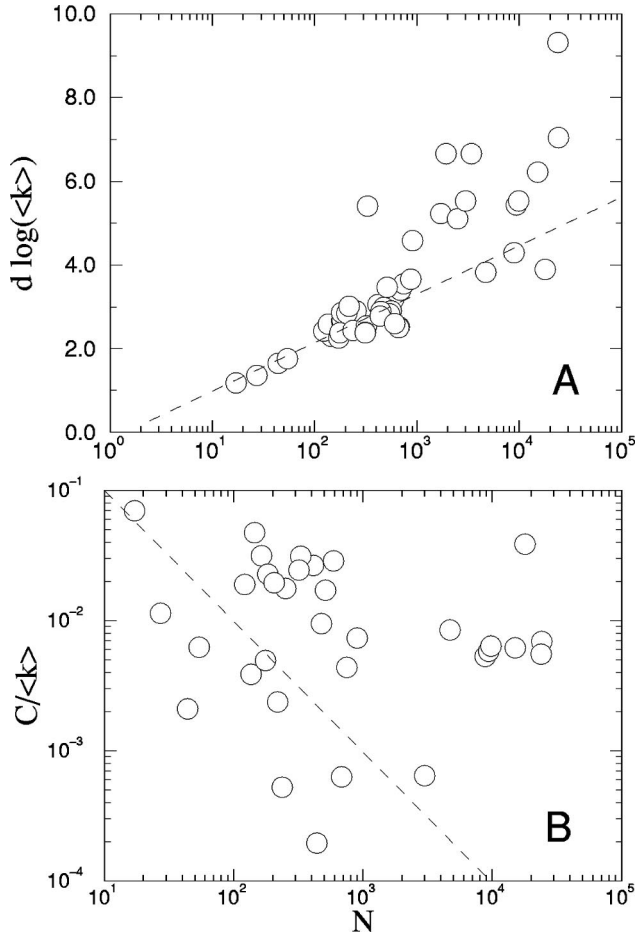


FIG. 4. Small world patterns in networks: distance (a) and clustering (b) for the circuits in the ISCAS'89/ITC'99 are shown. Real distance is corrected by a factor of $\log\langle k \rangle$ and clustering by $\langle k \rangle$. Dashed lines correspond to the values expected for random graphs, i.e., $C^{rand}/\langle k \rangle$ and $d^{rand} \log\langle k \rangle$, respectively. It can be seen that larger circuits involve larger deviations from the random cases.

magnitude are achieved by the largest circuits while d/d^{rand} remains in the same order of magnitude for whatever size of the network. There are some exceptions to $C/C^{rand} > 1$ which can be attributed to the fact that the ISCAS'89/ITC'99 sets are intended as benchmarks. In this respect, a reduced number of circuits are not described at the lowest level, and some others have been modified with the insertion of extra components. These two factors are likely to reduce clustering.

Nonetheless, the small-worldness of the circuits increases with the size of the circuit. From the industrial point of view, technological advance allowed circuits to grow in size. As the size increased, building circuits from scratch became unapproachable. It thus became necessary to build complex circuits using other basic circuits. On the one hand, these basic circuits have a reduced number of inputs and output wirings in comparison with their internal connections, so they are likely to be responsible for the high values of clustering observed. On the other hand it is known that a small number of wires interconnecting highly clustered units (according to Watt's model [2]) is enough for showing the small-world phenomenon at the high level.

III. DISCUSSION

Design of electronic circuits is divided into logical design and physical design [22]. The former specifies the network (components and connections), and the latter specifies the precise physical realization of the system in a particular technology. Optimization is present at both stages. Automatic methods of algebraic simplification are responsible for obtaining circuits having a minimal number of components in the logic design [23] (for optimization at the physical level, see Ref. [22]). This simplification is likely to be the origin of the low clustering attained in one half of the circuits analyzed. Simplified combinatorial circuits have the form of hierarchical networks (propagating inputs to the output without backward connections), which might explain such low clustering. It has been shown that if vertices in a network are physically placed on a ring, minimizing the logic distance (the distance between vertices in the graph) and the physical distance (the Euclidean distance between vertices) leads to small-world patterns [24].

Electronic circuits constitute an example of manmade artifacts that have evolved towards nonrandom configurations in which minimization of both average path length and physical distance are present. Because of their particular design, standard electronic devices are highly error prone: a single failure in one component typically leads to system failure. This is not the case of biological systems, in which networks displaying highly heterogeneous degree distributions with long tails have been shown to be particularly resilient [15]. Of course the difference comes largely from the *dynamical* pattern of interactions among units. Redundancy and modularity can help to overcome failure of a single unit by finding appropriate pathways able to substitute the damaged unit. Is there any analogous scenario within our context?

How reliable systems can be built from unreliable components has been a very important topic since Von Neumann's [25] and McCulloch [26] pioneering work. Using formal approaches borrowed from automata theory and statistical mechanics, these authors concluded that some amount of redundancy is required in order to satisfy a number of lower bounds of system functioning. One interesting framework in which our results might help to provide new ways of generating reliable circuits is the emerging area of adaptive and evolutionary hardware [27,28]. A new generation of electronic devices is based on the possibility of reconfiguration of the circuits wiring [29]. Self-reconfiguration is needed to endow devices with the flexibility of *in situ* challenges and an adaptation to unforeseen conditions, that also possess an enhanced fault tolerance. This is the case, for example, of planetary space missions.

The idea behind the evolutionary synthesis of electronic circuits is to employ an evolutionary and genetic algorithm to control the search for a circuit (through a potentially vast parameter space) that satisfies specified objectives. The evolutionary algorithm selects a population of potential designs, coded as bit strings configurations, and downloads them to the reconfigurable chip. Evolved circuits can have some flexibility which might allow them to work safely under different

sources of noise or damage. One possible constraint to be introduced into an evolutionary search would be inspired by the properties displayed by biological systems showing a SW topology. Searching for circuits with SW structure and/or long-tailed distributions of links might give some new insight into the origins of the SW behavior in both natural and artificial systems. The fact that the observed degree distributions of real designs are already power laws allows one to conjecture the possibility of reaching high levels of robust-

ness against the random failure of units under an appropriate level of redundancy.

ACKNOWLEDGMENTS

We are grateful to Emília Gutiérrez for providing us with the analogic circuits in Ref. [17,18]. This work was supported by the Santa Fe Institute (R. V. S.) and grants of the Generalitat de Catalunya (FI/2000-00393, R. F. C.) and the CICYT (PB97-0693, R. V. S.).

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- [29] An example of evolvable hardware is an adaptive configurable electronic circuit, such as a field programmable gate array (FPGA). An FPGA is an array of logic blocks (analogous to cells) placed in an infrastructure of interconnections, which are programmed at three distinct levels: the function of the logic cells, the interconnections between cells, and the inputs and outputs to the system. FPGA's exhibit an online adaptation by configuring their architecture dynamically and autonomously.